IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Baily, et al.	Docket No.:	ROC920030218US1
Serial No.:	10/616,683	Group Art Unit:	2112
Filed:	07/10/03	Examiner:	Stiglic, Ryan M.

For: COMPUTER APPARATUS AND METHOD FOR AUTONOMICALLY DETECTING SYSTEM CONFIGURATION AND MAINTAINING PERSISTENT I/O BUS NUMBERING

APPEAL BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This appeal is taken from the Examiner's final rejection, set forth in the Office Action dated 11/10/05. Applicants' Notice of Appeal under 37 C.F.R. § 1.191 was mailed on 2/10/2006.

REAL PARTY IN INTEREST

International Business Machines Corporation is the Real Party in Interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for this patent application.

STATUS OF CLAIMS

Claims 1-20 were originally filed in this patent application. Claim 16 was amended and claims 17-18 were cancelled. In the pending final office action, claims 1-16 and 19-20 were rejected. No claim was allowed. Claims 1-16 and 19-20 are currently pending.

STATUS OF AMENDMENTS

In response to a first office action an amendment was filed on 9/10/2005. After the final rejection dated 11/10/2005, a Notice of Appeal was timely filed on 2/10/2006, and this Appeal Brief is also being timely filed. Therefore, the claims at issue in this appeal are the claims as amended by the amendment filed 9/10/05.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 recites an apparatus with a non-volatile memory that contains bus numbering information (Figure 6, 622) for a bus located within a first apparatus (Figure 6, 620) and bus numbering information (Figure 6, 632) for a bus located in a second apparatus (Figure 6, 630).

Claim 4 recites a computer system with a first physical enclosure (Figure 6, 620) and a second physical enclosure (Figure 6, 630) that includes a non-volatile memory (Figure 6, 632) that contains bus numbering information for buses located within the first and second physical enclosures (Figure 6, contents of 632), and a bus number manager

that detects a change in configuration of the computer system (page 16, lines 19-25) and reads the bus numbering information from the non-volatile memory to determine an appropriate bus number (page 11, lines 16-25).

Claim 7 recites a computer systems with multiple physical enclosures (Figure 6, 110, 620, 630). The first physical enclosure (Figure 6, 110) includes a bus number mask (Figure 6, contents of 112) that indicates bus numbers in use in the computer system. The second and third physical enclosures (Figure 6, 620, 630) have at least one numbered bus and a non-volatile memory that has bus numbering information for the local enclosure and bus numbering information for another enclosure (Figure 6, 622, 632), and a bus number manager that detects a change in configuration of the computer system (page 16, lines 19-25) and reads the bus numbering information from the non-volatile memory to determine an appropriate bus number (page 11, lines 16-25).

Claim 9 recites a computer implemented method (Figure 8, 800) that includes assigning bus numbers for buses in multiple physical enclosures (Figure 6, 622, 632) and then storing bus numbers in a non-volatile memory in the enclosures (Figure 8, 860).

Claim 12 recites a computer implemented method (Figure 8, 800) that includes storing bus numbers in a non-volatile memory in multiple physical enclosures (Figure 6, 622, 632), detecting a change in the computer configuration and reading the bus numbering information from non-volatile memory (Figure 8, 820) to determine an appropriate bus numbering for at least one bus in the physical enclosures (Figure 8, 840).

Claim 14 recites a computer implemented method (Figure 8, 800) that includes assigning bus numbers for buses in multiple physical enclosures (Figure 6, 622, 632) then storing bus numbers in a non-volatile memory in multiple physical enclosures (Figure 6, 622, 632), detecting a change in the computer configuration, and then reading the bus

numbering information from non-volatile memory (Figure 8, 820) to determine an appropriate bus numbering for at least one bus in the physical enclosures (Figure 8, 840).

Claim 16 recites a program product comprising a bus number manager that detects a change in configuration of the computer system (page 16, lines 19-25) and reads the bus numbering information from the non-volatile memory to determine an appropriate bus number (page 11, lines 16-25)

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The following single ground of rejection is presented for review on this Appeal:

1. **Whether claims 1-16 and 19-20 are unpatentable under 35 U.S.C. §103(a) over applicant's admitted prior art (AAPA) in view of Mizukami (US 2002/0120708A1).**

ARGUMENT

Issue 1: Whether claims 1-16 and 19-20 are unpatentable under 35 U.S.C. §103(a) over applicant's admitted prior art (AAPA) in view of Mizukami (US 2002/0120708A1).

The Examiner rejected claim 1 as being unpatentable over AAPA in view of Mizukami. Applicant traverses the Examiner's finding of obviousness of claims 1-16 and 19-20. The cited art individually or in combination does not teach or suggest the claimed invention herein.

Mizukami teaches a node information management system for a communications network communicating between network nodes. Each node has node information that is stored in volatile memory. Node information is also stored in adjacent nodes such that if node information is lost, it can be restored from adjacent nodes. Mizukami teaches node information includes communication quality information, information regarding the user and node setting information [0006]. The first two of these are clearly not related to bus numbers. Node setting information is described in more detail in paragraphs [0032] and [0211]. Node setting information includes routing information and transfer information [0032]. Other examples of node information include elements such as occupation band, connecting time, and charge for the user [0211]. In each case, the node setting information does not read on bus numbering information. Mizukami teaches to store information in volatile memory that can be used to overcome operational errors.

In contrast, the claimed invention is concerned with a computer system located in multiple physical enclosures. Each of the enclosures has a non-volatile memory (NVRAM) that contains information about what buses are located in the enclosure. The claimed invention is directed to bus numbering information stored in the NVRAM for buses located in a different enclosure (apparatus).

Claims 1-3, 7-11

The combination of the AAPA and Mizukami does not teach or suggest the invention in claim 1 without hindsight provided by Applicant's disclosure. There is nothing in Mizukami to suggest to one of ordinary skill in the art to modify the AAPA in the manner proposed by the Examiner. A proper combination of Mizukami with the AAPA would merely teach overcoming loss of communication information stored in volatile memory by storing the communication information in adjacent nodes of a communications network that includes computers that have multiple physical enclosures. Mizukami does not teach or suggest anything about storing bus numbering information in non-volatile memory in a second apparatus. The idea of storing bus numbering information in the non-volatile memory of a coupled computer apparatus is not evident from the combination, this extension of the combination is only evident using hindsight reconstruction.

Further evidence of the use of hindsight reconstruction is revealed by the level of abstraction the Examiner used to characterize the cited art and the invention. The Examiner's rejection used a "failure event" to find similarities between the cited art and the claimed invention. There is no "failure event" in the claim language. Similarly, the Examiner's rejection uses a "node" to equate a communication node in Mizukami to an apparatus (enclosure of a computer in other claims). These broad characterizations of Mizukami and the claim language only make sense when one is familiar with the Application herein. Since the Examiner's rejections is based on inappropriate hindsight re-construction, Applicant respectfully requests that the Examiner's final rejection under 35 U.S.C. §103(a) be reversed

Further, even if the combination does teach the claimed invention, there is no motivation to combine the cited art. Mizukami is concerned with preserving node data in a communication system due to a power loss in one node or due to lost packet

information. The problem in Mizukami is solved by storing information in volatile memory. The claimed invention is concerned with bus numbering information for hardware configuration that is stored in the non-volatile memory of a second apparatus. This is not the same concern as shown in Mizukami. The loss of bus numbering information is due to hardware being changed. There is nothing to suggest to one of ordinary skill in the art that the method of preserving data from a failure in a volatile memory system of Mizukami would solve the problem of non-volatile memory bus information that is lost due to equipment change. The environment, computer system and problems in Mizukami are completely different than the computer systems, equipment and problems solved by the claimed invention. The precedent is clear that there must be some motivation evident from the cited art to combine references for a obviousness rejection. There is no such motivation evident in Mizukami.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) Mizukami and the AAPA have different areas of concern. There is nothing to suggest the desirability of combining the AAPA with Mizukami to in the manner of the claimed invention. The courts have consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed. See, e.g., In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."). The Examiner's stated motivation to combine is: "such that the possibility of configuration data (bus numbering information) is lost can be reduced even if a failure occurs in a particular device". In the claimed invention, the loss of information is not associated with a failure. Thus the Examiner's stated motivation to combine AAPA and Mizukami is defective since it does not suggest to combine the art in the manner of the claimed invention.

The examiner's motivation to combine (as quoted above) may appear to be derived from Mizukami, but the stated motivation to combine is a conclusion by the Examiner derived from the applicant's disclosure. The Examiner's motivation to combine requires a substitution of configuration information taught by Mizukami with hardware bus numbering information. As described above, configuration information in Mizukami is does not even resemble bus numbering. There is nothing to teach or suggest to substitute the operational bus configuration information with hardware configuration type information such as bus numbering information. This substitution is not supported in the cited art and is conclusory by the Examiner. The claim term of "bus numbering information" does not read on "configuration data" used in Mizukami. Absent hindsight reconstruction using the applicant's disclosure for a roadmap, there is no teaching in the cited art to characterize the motivation to combine the cited art as stated by the Examiner.

A proper motivation to combine Mizukami and AAPA would be one to get the advantages of Mizukami in the environment of the AAPA. Without reading the applicant's disclosure, which characterizes the prior art in a specific way to introduce the improvement of the applicant's invention, one of ordinary skill in the art would not be motivated to combine the AAPA with Mizukami in the manner indicated by the Examiner. The AAPA does not include the careful characterization of the limitations of the prior art in the Applicant's disclosure. Apparently the Examiner has used this characterization of the prior art limitations portion of the AAPA to build a motivation to combine. In contrast, a proper characterization of the motivation to combine Mizukami and AAPA would be to achieve a simple combination as described above, namely, a communications network that includes computers that have multiple physical enclosures with configuration data in the volatile memory of adjacent nodes in case of loss from an operational type failure. The motivation for this combination would be to manage node information to overcome a communications failure. Any further extension of the motivation to combine includes the improper conclusions drawn from hindsight of the Applicant's disclosure.

Since AAPA in view of Mizukami does not teach or suggest to store bus numbering information in the non-volatile memory of a second apparatus, therefore AAPA in view of Mizukami does not teach or suggest claim 1, and applicants respectfully request that the Examiner's final rejection of these claims under 35 U.S.C. §103(a) be reversed.

Claims 2 and 3 depend on claims 1, which are allowable for the reasons given above. As a result, claims 2 and 3 are also allowable as depending on an allowable independent claim. Applicants respectfully request that the Examiner's final rejection of claims 2 and 3 under 35 U.S.C. §103(a) be reversed.

Independent claims 7 and 9 include similar limitations as discussed above for claim 1. The arguments above with respect to claim 1 apply equally to claims 7 and 9, and are incorporated in this section by reference. Claims 8 and 10-11 depend on claims 7 and 9 respectively, which are allowable for the reasons given above. As a result, claims 8 and 10-11 are also allowable as depending on an allowable independent claim. Applicants respectfully request that the Examiner's final rejection of claims 2 and 3 under 35 U.S.C. §103(a) be reversed.

Claim 4-6, 12-16, 19 and 20

The arguments above with respect to claim 1 apply equally to claims 4-6, 12-16, 19 and 20, and are incorporated in this section by reference. Further, with regards to claim 4 and the claim limitation of "a bus number manager that detects a change in configuration of the computer system and that reads the bus numbering information from non-volatile memory", the Examiner cited AAPA; Figures 1-5, items 122, 133, 142 or 152; and page 5, lines 3-18. The cited sections describe the prior art method of

configuring the buses in the system. The AAPA teaches to detect an invalid configuration and configure the bus with new bus numbering. In contrast, in claim 4, a change in the configuration is detected and then the bus numbers are assigned accordingly by looking to the bus numbers stored in the neighboring towers (page 14, lines 14-18). The prior art system would assign the bus numbering without regard to the previous configuration. Since the cited art does not teach or suggest a "a bus number manager that detects a change in configuration of the computer system and reads the bus numbering information from the non-volatile memory", applicant's respectfully request that the Examiner's final rejection of these claims under 35 U.S.C. §103(a) be reversed.

Claims 5 and 6 depend on claims 4, which is allowable for the reasons given above. As a result, claims 5 and 6 are also allowable as depending on an allowable independent claim. Therefore the cited art does not teach or suggest claims 5 and 6, and applicants respectfully request that the Examiner's final rejection of claims 5 and 6 under 35 U.S.C. §103(a) be reversed.

Independent claims 12, 14 and 16 include similar limitations as discussed above for claim 4. The arguments above with respect to claim 4 apply equally to claims 12, 14 and 16, and are incorporated in this section by reference. Claims 13, 15, 16 and 19-20 depend on claims 12, 14, and 16 respectively, which are allowable for the reasons given above. As a result, claims 13, 15, 16 and 19-20 are also allowable as depending on an allowable independent claim. Applicants respectfully request that the Examiner's final rejection of claims 12-16 and 19-20 under 35 U.S.C. §103(a) be reversed.

CONCLUSION

Claims 1-16 and 19-20 are addressed in this Appeal. For the numerous reasons articulated above, applicants maintain that the rejections of claims 1-16 and 19-20 under 35 U.S.C. § 103(a) are erroneous.

Applicants respectfully submit that this Appeal Brief fully responds to, and successfully contravenes, every ground of rejection and respectfully requests that the final rejection be reversed and that all claims in the subject patent application be found allowable.

Respectfully submitted,

/bretjpetersen/
Bret J. Petersen
Reg. No. 37,417

MARTIN & ASSOCIATES, L.L.C.
P.O. Box 548
Carthage, MO 64836-0548
(417) 358-4700
Fax (417) 358-5757

CLAIMS APPENDIX

1. A first apparatus comprising:
a non-volatile memory that contains:
(A) bus numbering information for at least one bus located within the first apparatus; and
(B) bus numbering information for at least one bus located within a second apparatus coupled to the first apparatus.

2. The first apparatus of claim 1 wherein the bus numbering information comprises a beginning bus number and a number of buses.

3. The first apparatus of claim 1 wherein the non-volatile memory comprises at least one identifier for determining if contents of the non-volatile memory are valid.

4. A computer system comprising:

a first physical enclosure;

a second physical enclosure coupled to the first physical enclosure, the second physical enclosure including a non-volatile memory that contains bus numbering information for buses contained in the first and second physical enclosures; and

a bus number manager that detects a change in configuration of the computer system and that reads the bus numbering information from the non-volatile memory for the first and second physical enclosures to determine an appropriate bus number for at least one bus in the first and second physical enclosures.

5. The computer system of claim 4 wherein the bus numbering information comprises a beginning bus number and a number of buses.

6. The computer system of claim 4 wherein the non-volatile memory comprises at least one identifier that is read by the bus number manager to determine if contents of the non-volatile memory are valid.

7. A computer system comprising:

(1) a first physical enclosure comprising:

at least one processor;

a memory coupled to the at least one processor;

a non-volatile memory coupled to the at least one processor, the non-volatile memory including a bus number mask that indicates bus numbers in use in the computer system; and

a hub coupled to the at least one processor;

(2) a second physical enclosure comprising:

at least one bridge coupled to the hub in the first physical enclosure;

at least one numbered bus coupled to the at least one bridge;

a non-volatile memory that contains:

(A) bus numbering information for numbered buses in the second physical enclosure; and

(B) bus numbering information for numbered buses in a third physical enclosure;

(3) the third physical enclosure comprising:

at least one bridge coupled to the at least one bridge in the second physical enclosure;

at least one numbered bus coupled to the at least one bridge in the third physical enclosure;

a non-volatile memory that contains:

(A) bus numbering information for numbered buses in the third physical enclosure; and

(B) bus numbering information for numbered buses in the second physical enclosure;

(claim 7 continued)

(4) a bus number manager residing in the memory of the first physical enclosure and executed by the at least one processor in the first physical enclosure, the bus number manager detecting a change in configuration of the computer system and reading the bus numbering information from the non-volatile memory in the second and third physical enclosures to determine an appropriate bus number for at least one bus in the second and third physical enclosures.

8. The computer system of claim 7 wherein the bus numbering information comprises a beginning bus number and a number of buses.

9. A computer-implemented method for storing bus numbering information in a non-volatile memory, the method comprising the steps of:

assigning unique bus numbers to buses in a first physical enclosure;

assigning unique bus numbers to buses in a second physical enclosure; and

storing the bus numbers for the buses in the first and second physical enclosures in the non-volatile memory.

10. The method of claim 9 wherein the non-volatile memory resides in the first physical enclosure.

11. The method of claim 9 wherein the bus numbering information comprises a beginning bus number and a number of buses.

12. A computer-implemented method for numbering a plurality of buses in a computer system that includes a plurality of physical enclosures, the method comprising the steps of:

storing in a non-volatile memory bus numbering information for at least one bus in a first physical enclosure;

storing in the non-volatile memory bus numbering information for at least one bus in a second physical enclosure;

detecting a change in the computer system configuration; and

reading the bus numbering information from the non-volatile memory for the first and second physical enclosures to determine an appropriate bus number for at least one bus in the first and second physical enclosures.

13. The method of claim 12 wherein the bus numbering information comprises a beginning bus number and a number of buses.

14. A computer-implemented method for assigning and maintaining persistent numbers to a plurality of buses in a computer system that includes a plurality of physical enclosures, the method comprising the steps of:

assigning unique bus numbers to buses in a first physical enclosure;

assigning unique bus numbers to buses in a second physical enclosure coupled to the first physical enclosure;

storing bus numbering information corresponding to the bus numbers for the buses in the first and second physical enclosures in a first non-volatile memory in the first physical enclosure;

storing bus numbering information corresponding to the bus numbers for the buses in the first and second physical enclosures in a second non-volatile memory in the second physical enclosure;

detecting a change in the computer system configuration;

reading the bus numbering information from the first and second non-volatile memories to determine an appropriate bus number for the buses in the first physical enclosure; and

reading the bus numbering information from the first and second non-volatile memories to determine an appropriate bus number for the buses in the second physical enclosure.

15. The method of claim 14 wherein the bus numbering information comprises a beginning bus number and a number of buses.

16. A program product comprising:

a bus number manager that detects a change in configuration of a computer system that includes a plurality of physical enclosures, the bus number manager reading bus numbering information from a non-volatile memory in a first physical enclosure to determine an appropriate bus number for at least one bus in the first physical enclosure and at least one bus in a second physical enclosure; and

recordable signal bearing media bearing the bus number manager.

17. (Cancelled)

18. (Cancelled)

19. The program product of claim 16 wherein the bus numbering information comprises a beginning bus number and a number of buses.

20. The program product of claim 16 wherein the non-volatile memory comprises at least one identifier that is read by the bus number manager to determine if contents of the non-volatile memory are valid.